

ABSTRACT

The invention concerns an image-forming apparatus employing a clock-generating circuit, which generates dot clock pulses utilized for an image-writing section of the image-forming apparatus. The clock-generating circuit includes a digital-delay dot clock adjusting section to generate first dot clock pulses having a predetermined number of pulses within a predetermined time interval at a constant exposing range of the image-writing section, wherein each period of the first dot clock pulses is slightly increased or reduced by changing a selection for a plurality of delayed clock pulses, which are generated by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times; and a jitter suppressing section to suppress a jitter component included in the first dot clock pulses, wherein the jitter suppressing section divides the first dot clock pulses to generate second dot clock pulses, and then, multiplies the second dot clock pulses to generate the dot clock pulses.